2 ~~45~~. The memory circuit as claimed in claim 1 ~~43~~, said delay circuit comprising a shift-register.

6 ~~48~~. The memory circuit as claimed in claim 5 ~~44~~, said delay circuit comprising a shift-register.

3 ~~47~~. The memory circuit as claimed in claim 1 ~~43~~, said delay circuit receiving latched address signals latched by the address-input circuit.

4 ~~48~~. The memory circuit as claimed in claim 3 ~~47~~, said delay circuit delaying the latched address signals for 1.5 clock cycles.--

REMARKS

Please charge any fee deficiency or credit any overpayment to Deposit Account No. 01-2300.

Respectfully submitted,

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